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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Sheet 1 of 1

Complete if Known	
Application / Conf. No.	~~Unknown~~ 10/792,153
Filing Date	March 02, 2004
First Named Inventor	Robert E. Eccles
Art Unit	~~Unknown~~ 2825
Examiner Name	~~Unknown~~ P. RIK
Attorney Docket Number	X-1270 US

OTHER – NON PATENT LITERATURE DOCUMENTS

Examiner Initials *	Cite No[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
PR		Xilinx, Inc.; Application Note, XAPP108; "Chip-Level HDL Simulation Using the Xilinx Alliance Series"; May 21, 1998 (Version 1.0); available from Xilinx, Inc., 2100 Logic Drive, San Jose, California 95124; pp. 1-15	
PR		Altera; Application Note 296; "Using Verplex Conformal LEC for Formal Verification of Design Functionality"; January 2003, Ver. 1.0; available from Altera Corporation; pp. 1-14.	
PR		Xilinx, Inc.; Application Note, XAPP413; "Xilinx/Verplex Conformal Verification Flow"; October 2, 2001 (Version 1.1); available from Xilinx, Inc., 2100 Logic Drive, San Jose, California 95124; pp. 1-10	
PR		Xilinx, Inc.; Application Note, XAPP414; "Xilinx/Synopsys Formality Verification Flow"; January 21, 2002 (Version 1.3); available from Xilinx, Inc., 2100 Logic Drive, San Jose, California 95124; pp. 1-15	
PR		IEEE Verilog(TM) HDL Language Reference Manual Project (LRM); Chapter 7.6; downloaded from http://www-ee.eng.hawaii.edu/~msmith/ASICs/HTML/Verilog/Verilog.htm; February 24, 2004; pp. 1-14.	
PR		Xilinx, Inc.; Table 2-1 "Design Verification"; downloaded from http://toolbox.xilinx.com/docsan/xilinx5/data/docs/dev/dev0015_6.html; February 28, 2003; pp. 1-9.	

Examiner Signature		Date Considered	3/24/06

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[1] Applicant's unique citation designation number. [2] Applicant is to place a check mark here if English language Translation is attached.

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